Hall Ticket Number:

Code No. : 14468 AS AO

VASAVI COLLEGE OF ENGINEERING *(AUTONOMOUS)*, HYDERABAD

Accredited by NAAC with A++ Grade

B.E. (E.C.E.) IV-Semester Advanced Suppl. Examinations, Aug./Sep.-2023

Digital System Design

Time: **3 hours** Max. Marks: **60**

*Note: Answer all questions from **Part-A** and any **FIVE** from **Part-B***

Part-A (10× 2 = 20 Marks)

Q. No.	Stem of the question	M	L	CO	PO
1.	Write the expression to identify minterms 0,2,4,6 in SOP form.	2	1	1	1
2.	Express the Decimal Digits 45.45 in Binary and Octal Numbers.	2	2	1	2
3.	Construct XOR gate using only NAND gates.	2	1	2	1
4.	Write the Truth Table of a 2x4 Decoder.	2	1	2	1
5.	List the differences between Counters and Registers.	2	2	3	1
6.	Draw the symbol and Truth Table of JK Flip Flop.	2	1	3	1
7.	Identify the difference data types used in Verilog HDL.	2	1	4	1
8.	Write Verilog HDL code for AND & OR gates.	2	1	4	1
9.	Define Gate Level Net List.	2	1	5	1
10.	Mention any Two applications of FPGA.	2	1	5	1
	Part-B (5×8 = 40 Marks)				
11. a)	Simplify F = xyz + x'y + xyz' and draw circuit using Basic Gates.	4	3	1	2
b)	Determine the minimal expression for the following Boolean function using K-Map method: F(A,B,C,D)=∑(1,3,4,11,12,13,15).	4	3	1	2
12. a)	Design 1-bit Full Adder using Two Half Adders.	4	3	2	2
b)	Design a 4x1 Multiplexer using 2X1 Multiplexer.	4	3	2	2
13. a)	Mention any 4 differences between Combinational and Sequential circuits.	5	4	3	3
b)	Draw the circuit of 4 bit Ripple Counter and explain its working.	4	2	3	2
14. a)	Write the Verilog code for 2 bit Comparator in Gate Level Modeling.	4	2	4	3
b)	Explain the role of Compiler Directives in Verilog HDL.	4	2	4	1

Conta... 2

15. a)	Identify different Blocking and Non Blocking Assignment statements and give example to each of them.	4	4	5	1
b)	Draw the Flow chart of Logic Synthesis.	4	4	5	
16. a)	Explain about 8421 and Excess 3 Codes.	4	2	1	2
b)	Design a 4 bit Gray to Binary Code converter and circuit diagram.	4	3	2	3
17.	Answer any ***two*** of the following:				
a)	Describe the operation of Pseudo Random Sequence Generator.	4	2	3	1
b)	Explain significance of Test bench in simulation.	4	2	4	1
c)	Drae the Block Diagram of FPGA and explain it.	4	2	5	1

M : Marks; L: Bloom's Taxonomy Level; CO; Course Outcome; PO: Programme Outcome

i)	Blooms Taxonomy Level – 1	20%
ii)	Blooms Taxonomy Level – 2	40%
iii)	Blooms Taxonomy Level – 3 & 4	40%

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